Design of Transistor Level Circuit for Cosine Wave Mapping Function: Applied to Dynamics Models

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Abstract. This brief focuses on the design of analog circuits generating a trigonometric mapping function, such as the cosine function. The designed mapping circuit is to be used as a core component for a circuit emulating the non linear behavior such PVTOL (Planar Vertical Take-Off and Landing). With the analog solution for trigonometric synthesis functions the designer expects a continuous time response with no quantization error. In order to test the proposed approach, the vertical dynamics of a PVTOL system is emulated.

Keywords: Aircraft, Dynamic Model, Nonlinear Systems, Electronic Applications, Circuits Design, Nonlinear Equations, Continuous time systems.

1 Introduction

In the late 1970s and early 1980s "analog" was considered obsolete, anyone seriously contemplating the analog design was out of the modern age of electronic circuit design. This view changed abruptly with the ASIC revolution of the mid-1980s. Indeed, much analog did migrate into some digital form [1] and [2] .

Even today more than ever are becoming more functions and problems working with microcontrollers, microprocessors and useful devices for processing digital signals.

However the higher the amount of digital systems which are created for the data acquisition and process control interface circuits also more internally using analog circuits to operate at a continuous rate as in the case of high speed dividers are required, emulators for real-time control, analog processors focused on the area of the image, signal generators, etc... [3] , [4], [5], [6], [7]. To design embedded circuits, designers must understand the basic principles of analog design. This is to achieve a good performance at a reasonable cost [8].

This paper mainly focuses on the generation of cosine trigonometric function, noticing the problematic that has in certain analog solution analyzed mostly in the control area with non-linear models, such as VTOL (Vertical Take-off and Landing) and PVTOL (Planar Vertical Take-Off and Landing) nonlinear systems

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whose mathematical models involve trigonometric functions [9], [10], [11] and [12] which are currently mostly simulated digitally. We will focus mainly on the PVTOL model presented in [9].

PVTOL Dynamic Model The following model is proposed for the simplified description of the dynamics of a PVTOL system.

$$\ddot{x} = -u_1 sin(\theta) + \epsilon u_2 cos(\theta) \tag{1}$$

$$\ddot{y} = u_1 cos(\theta) + \epsilon u_2 sin(\theta) - 1 \tag{2}$$

$$\ddot{\theta} = u_2 \tag{3}$$

Where "-1" is the gravitational acceleration and the variable ϵ is the (small) coefficient giving the coupling between the rolling moment and the lateral acceleration of the aircraft. Note that $\epsilon > 0$ means that applying a (positive) moment to roll left produces an acceleration to the right (positive x).

This simplified model is useful because particularized PVTOL system dynamics to a system of two controls that are taken as inputs which are u_1 and u_2 represent the thrust (upward direction) and angular acceleration (rolling moment or torque). As a result three outputs are considered: θ, x and y.

To model this simplified mathematical description on a digital system it is necessary to map the previously mentioned parameters θ, x, y, u_1 and u_2 into the digital domain. This task will add quantization noise to the system provided using a high sampling rate. Also, consider the phenomenon of latency to emulate digitally mapping system. On the other hand, a continuous-time model is more related to the mathematical description of the aforementioned model.

1.1 Behavioral Analysis of Non-linear Model

The nonlinear behavioral model described above is presented in blocks as shown in the Fig. 1, simulation results will be presented later, in order to show that the approximation of the cosine function proposed in this paper provides excellent results in almost any non-linear model in which a cosine function is required.

In this paper we present a continuous time representation related to analog circuits which provide a real time and no quantized mapping circuits useful to construct an analog PVTOL emulator. With the analog solution of trigonometric functions expected of this type of analog emulators there drawback of quantization noise is completely avoided. In addition a continuous time response is achieved at minimum expenses. Therefore, the main contribution of this paper is to offer an alternative to the solution of dynamic systems using the analog processing with a nonlinear circuit to transistor level.

2 Methods to Synthesize an Analog Cosine Mapping Function.

Realization of the cosine function is not supposed to be a simple task, because it was looking good accuracy and the mathematical calculation of the function is

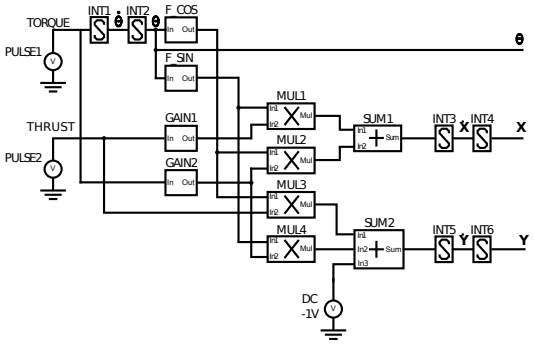


Fig. 1. Behavioral model blocks of PVTOL in Verilog-A

the least complex possible, this is as the main goal for analog circuit design is to obtain good accuracy with minimal resources . According to the literature studied were found at least 3 ways to do the cosine, one that is derived from series, the second is a proposed approximation very algebraically accurately analyzing the cosine function and the last method is a proposal that was implemented for the development of this work, appointed by approximation a nonlinear mapping.

In summary mode explained below each of these methods:

– Taylor:
The Taylor series is named in honor of the British mathematician Brook Taylor (1685-1731), is a representation of a function as an infinite sum of terms.
The approximation given an argument x is expressed as follows:

$$cos(x) = \sum_{n=0}^{\infty} (-1)^n \frac{x^{2n}}{2n!} ... \forall x \tag{4}$$

As the terms are increased it obtains a better approximation of the given function, cosine approximation with 4 terms can be seen in the Fig. 2. The measured error of the output waveform with respect to an ideal cosine function was $\pm 2.20\%$.

– Seevinck:
It is thus named in honor of the person who made this approximation implemented directly into electrical circuits using the translinear principle. Analyzing algebraically the cosine function, it obtain the equation 5.

$$cos(\pi x) = \frac{(1 - 4x^2)(2 - x^2)}{2 + x^2} \qquad -1 < x < 1 \tag{5}$$

The implementation of the cosine function using this approximation to transistor level is relatively simple, in addition, provides a very low $\pm 0.82\%$ error

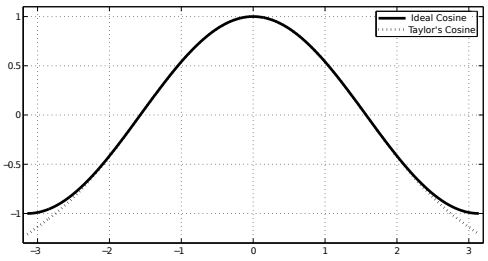


Fig. 2. Comparison of the approximation of cosine Taylor series and ideal cosine function

and is not restricted to rational functions. The author has implemented this approximation on a circuit designed for synthesizing cosine in [6].
An approximation of this equation is very good, as can be seen in the Fig. 3, that basically can not see any difference.

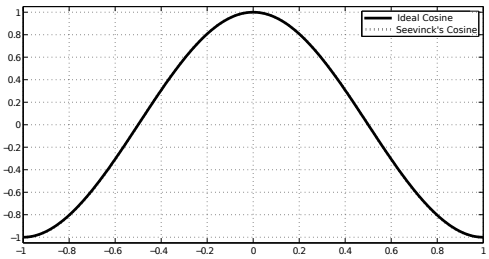


Fig. 3. Comparison of the approximation of cosine Seevinck and ideal cosine function

– The proposed non-linear mapping:
At difference of the techniques above mentioned, the technique proposed in the present work is based on the basic behavior of a MOSFET transistor and its response to certain inputs.
Thus, the implementation of this circuit is relatively simple and fully operational in voltage mode whit folding circuit. A detailed discussion is done in the next section.

The transistor level realization in analog form approximations by Taylor and Seevinck provide good results as shown in the previous figures, by Taylor approximation analog form in a circuit is a relatively difficult method because for a good approximation must be taken at least 4 terms and this mean that the design must be able to reach a sixth power, this requirement is difficult to achieve.

The approach Seevinck is not practical due to the resources required for its implementation, unlike the proposed method which requires few MOSFET transistors.

The goal of this paper is to find a new approach for the cosine function which is easy to implement to transistor level analyzing the behavior with the transfer function obtained at the output of a folding circuit without trying to implement some approximation formula directly, this novel design proposed called "Non-linear Mapping" will be explained more in detail in the next section ensuring relativity be a simple method for its implementation.

3 Implementation of the Non-linear Mapping Function to the Cosine.

3.1 Main Characteristics of the Cosine Function

To synthesize the cosine wave function it is important consider the periodicity, domain, the function is continuous throughout its domain, it is increasing function in the range [π, 2π] and decreasing in [0,π], that is even and the graph is symmetric with respect to the ordinate.

Among these features, it should be mentioned that the behavior in time to a period of -π to π of the cosine function is nonlinear, that is why we are working on the implementation as a nonlinear mapping for the approximation of the function.

At present the most circuits are performed in voltage mode, we can not forget this requirement, so another specification of our emulator circuit will be that works in voltage mode.

This is a advantage they face circuits in current mode, which usually require a voltage-current-voltage conversion so that, in terms of compatibility with the outside world, the technique of design in voltage mode is still present and quite important method [13].

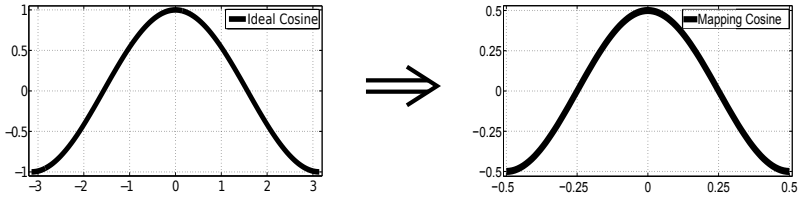
3.2 Circuit Implementation

The function of the mapping is to bring the values of the ideal cosine values as voltage at which the emulator will work, given that the technology implemented in this work is CMOS to 90nm, then the voltage values should range maximum of 1 volt on the Y axis or in amplitude, and instead of having a period of -π to π looking for a period of -0.5 to 0.5 as seen in the Fig. 4.

To perform this mapping, a technique called folding circuit will be used. This technique is based in the analysis of transfer function on that circuit.

A folding circuit implemented for the realization of a Gaussian is in [7]. the mistmach control circuit is shown in Fig. 5.

The topology with mismatch control [7] shown in the Fig. 5 will be used as part of the folding circuit proposed for this work, but in this case the number of transistors increases as the number of mismatch voltages in order to achieve



(a) Ideal cosine function (b) Mapping cosine function

Fig. 4. Objective mapping block cosine.

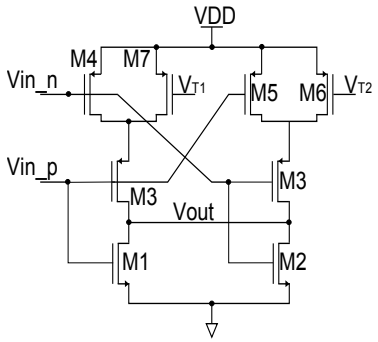


Fig. 5. Folding circuit with mismatch control.

a better fit of the signal and an optimal approximation of the desired function. Generalizing the cosine block that it will perform, this is divided internally into three sub-blocks, two main sub-block gain, and the folding circuit is performed can be seen in Fig. 6.

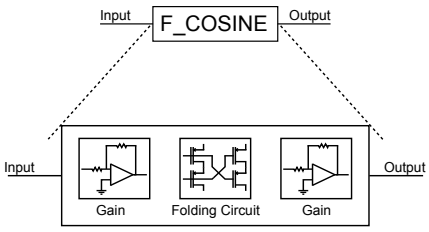


Fig. 6. General block cosine function.

In Fig. 7, we can see the folding circuit designed using standard 90 nm CMOS technology, having a pair of inputs fully differential, this means that when an entry is made low, the other input is set at a high level, both paths are switched off and the output voltage is zero. A true differential given level, the circuit begins

to conduct and output voltage starts to increase when the differential voltage is zero, the output reaches its maximum peak voltage, include the output (V_{out}) ends with a gain amplifier, this will help condition the signal amplitude required.

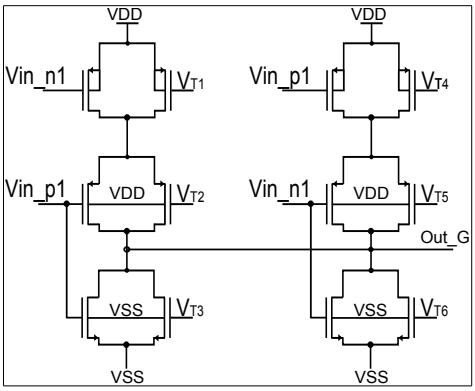
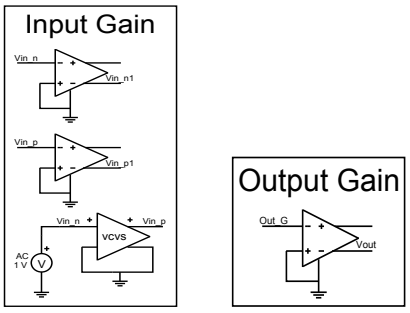


Fig. 7. Folding circuit for non-linear mapping.

To the input circuit (Vin_n1 y Vin_p1) also a pair of amplifiers are placed at certain gain as shown in Fig. 8, in order to adjust the output signal in the predetermined period.



(a) Gain to the input

(b) Gain to the output

Fig. 8. Gain block for fit end cosine function.

The final block of the cosine function by non-linear mapping approach is expressed in Fig. 9, where we can see the cosine mapping over a period of -0.5 to 0.5, as a dotted line and the approach to this mapping is emphasized by a solid line.

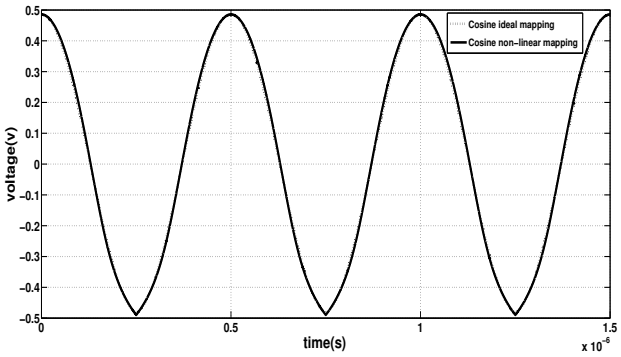


Fig. 9. Answer folding circuit.

This result (Fig. 9) demonstrates an alternative solution different to the digital process. It is important to mention what according the application will be the solution. Temperature variations can affect the circuit output for the moment this problem can be avoided with a temperature control, even so, the end is the real-time processing.

3.3 Electrical Parameters

Based in the file obtained for DC operating point simulation (Eldo-Spice), in the Tab. 1 shows current, voltage and consumption power values for the power supplies required for the MOSFETs of the folding circuit.

Table 1. General electrical parameters.

Source	**Current**	**Voltage**	**Power**
VSS	-3.5880mA	-500mV	-1.7940mW
VDD	-3.5880mA	500mV	-1.7940mW
V_{T1}	50nA	5.8mV	46.2066pW
V_{T2}	2.032nA	2mV	4.0640pW
V_{T3}	-856.9076pA	1.6mV	-1.3711pW
V_{T4}	6.1381nA	5.8mV	35.6010pW
V_{T5}	468.1643pA	2mV	936.3285pW
V_{T6}	-856.9076pA	1.6mV	-1.3711pW

4 Simulation Results.

In order to validate the results of the new approach of the cosine function mapped to transistor level, we will discuss only the vertical position of the system of

equations and the roll angle of the aircraft with the horizon, this means that in the system disappears the coupling between the rolling moment and the lateral acceleration of the aircraft ($\epsilon = 0$), therefore we obtain the following expressions:

$$\ddot{y} = u_1 cos(\theta) - 1 \tag{6}$$

$$\ddot{\theta} = u_2 \tag{7}$$

applying the system a control LQR, in Fig. 10 shows two responses in general . The solid lines (V(THETA)and V(Y)) are the responses on the system applying a cosine function mapping ideal, on the other hand the PVTOL system solutions represented by dotted lines (V(THETA_T)and V(Y_T)) are the responses obtained with the cosine block performed at transistor level and implemented within the model behavioral.

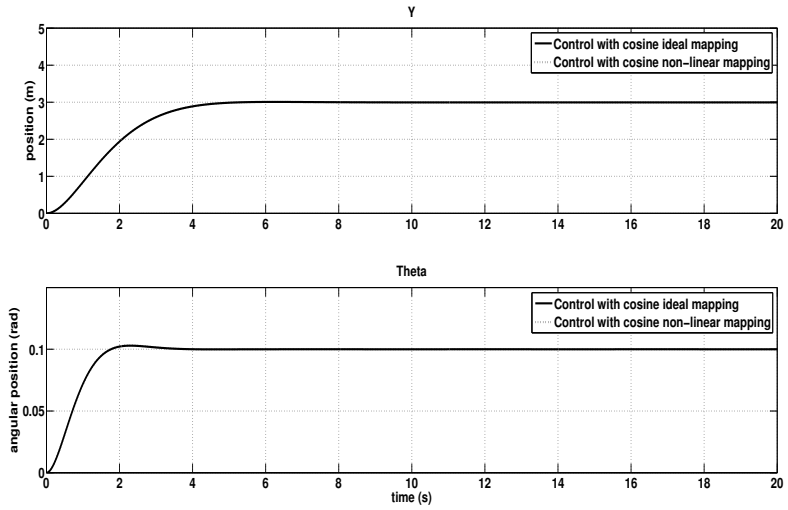


Fig. 10. Comparison of the original function mapping and transistor level function mapping

It is noteworthy that our new approximation will work correctly between the ranges of design to transistor level (-0.5 V to 0.5 V).

5 Conclusion

It is to be noted that this circuit produces very good results and a transistor level implementation has shown that it is relatively simple. All design was implemented using standard 90 nm CMOS technology and the measured error of the output waveform with respect to an ideal cosine function mapping was $\pm 1.14\%$.

As future work could implement a set of algebraic or trigonometric functions to transistor level with the technical folding proposed herein, emulating on a silicon chip presented any model of any system, better yet, making the the control on a chip, so that when the control is proved this can be done in continuous time but the model is very complex.

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